complete the Ph.D. degree. His Ph.D. thesis topic was "Radiation effects on power GaAs MESFET amplifiers." In 1982, he accepted a position in the R&D laboratory at Avantek, where he is responsible for design and development of GaAs MESFET monolithic microwave integrated circuits. He is presently a Senior Member of the Technical Staff.

Dr. Moghe has co-authored more than a dozen technical papers on GaAs MESFET characterization, radiation effects, and hybrid and monolithic microwave integrated circuits. He is a member of Sigma Xi.

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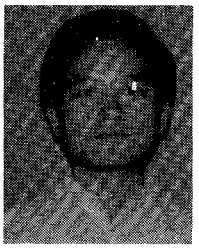

Horng-Jye Sun was born in Sze Chuan, China, on August 10, 1949. He received the B.S.E.E. and M.S.E.E. degrees from the National Taiwan University, Taipei, Taiwan, in 1971 and 1975, respectively, and the Ph.D. degree from Reneselaer Polytechnic Institute, Troy, NY, in 1982.

During 1971 to 1973, he was in the Navy of the Republic of China for Reserved Officer Service. In 1975, he joined the Chung Shan Institute of Science and Technology, Tau Yuan, Taiwan, where he worked as an assistant scientist on radar front-end receivers until 1979. From 1979 to 1982, he was a research assistant at Reneselaer Polytechnic Institute investigating optical effects in GaAs MESFET oscillators. His study has given some useful results on light-induced transient response and optical switching of GaAs MESFET oscillators. In 1982, he joined Avantek Incorporated, Santa Clara, CA, as a Member of the Technical Staff, where he has been working on the design and development of GaAs monolithic microwave integrated circuits.

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Capacitively Coupled Traveling-Wave Power Amplifier

YALCIN AYASLI, SENIOR MEMBER, IEEE, STEVEN W. MILLER, MEMBER, IEEE, ROBERT MOZZI, AND LARRY K. HANES

Abstract—**A new circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors is described. The approach is applied to a 1-W, 2–8-GHz monolithic amplifier design.**

I. Introduction

DISTRIBUTED or traveling-wave amplifiers covering wide microwave bands have been reported in recent years [1]–[5].

Designing a traveling-wave amplifier for maximum power, however, requires several additional considerations [6]. One is the limitation of input power. With a 50-Ω gate line and pinchoff voltages on the order of −4 V, the maximum power input is about 50 mW. A design allowing an increase in power input without sacrificing gain must be utilized.

In this paper, we present a circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors. Combined with the gate–source capacitance of the FET's, these capacitors act as voltage dividers, allowing us to sample a desired portion of the input signal from the gate line. In addition, by varying the divider ratio along the gate line, it is possible to tailor the input excitation to individual FET's. In this manner, the input power can be increased significantly (typically by a factor of four) and the total device periphery can be at least doubled. This should result in increased power output and efficiency.

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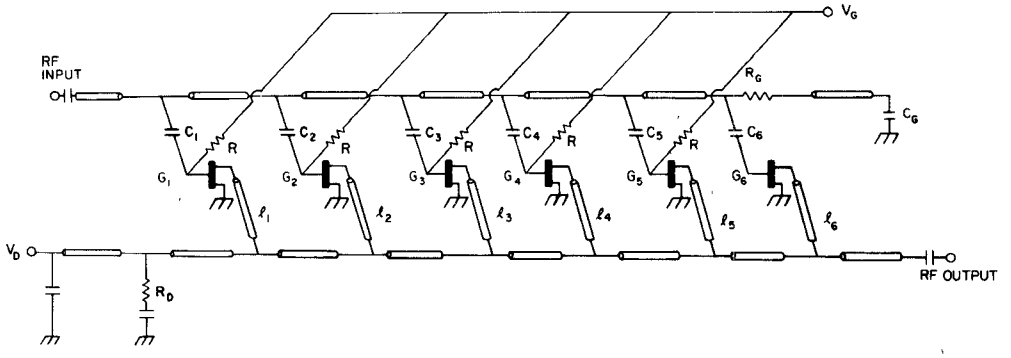

Fig. 1. Schematic circuit diagram of capacitively coupled traveling-wave amplifier.

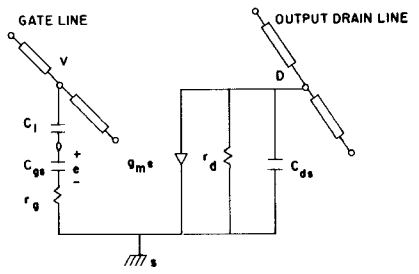

Fig. 2. The unit cell of Fig. 1.

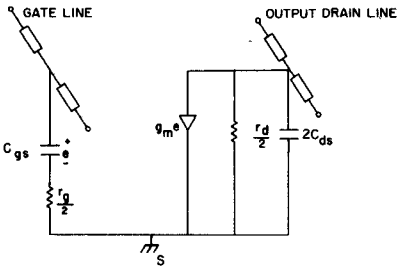

Fig. 3. The unit cell in Fig. 1 when the FET periphery is doubled and the thin-film capacitor C_1 set equal to the total gate-to-source capacitance.

II. General Design Considerations

The concept of capacitively coupling the individual FET's to the input gate line in a traveling-wave amplifier is illustrated in Fig. 1. Discrete thin-film capacitors are inserted in series with the FET gate terminals. If we approximate the input impedance of the FET by its gate capacitance, it is clear that we are forming a capacitive voltage divider and only a portion of the RF voltage excited in the input line will appear at the gate of the discrete FET's. This voltage division will be independent of frequency. Fig. 2 shows the simplified equivalent circuit diagram for the first cell.

From this figure, when $\omega C_{gs} r_g \ll 1$, the equivalent capacitance loading the gate line is

$$C_g = \frac{C_1 C_{gs}}{C_1 + C_{gs}}$$

and the voltage drop across the gate junction is

$$e = \frac{C_1}{C_1 + C_{gs}} V$$

for example, if $C_1 = C_{gs}$, then

$$C_g = C_{gs}/2$$

$$e = \frac{V}{2}.$$

The reduction in the voltage across the gate junction will result in this case in a 6-dB gain reduction for the overall amplifier. However, this can be compensated for by doubling both the periphery of the FET's and the value of C_1. If this is done, the equivalent circuit of Fig. 2 can be reduced to the circuit of Fig. 3. From this figure, we see that a new FET model, including the series capacitance C_1, can be defined. This new FET model is similar to the original FET we have started with, except for the gate and drain resistances, which are halved, and the drain–source capacitance, which is doubled.

This new circuit configuration, illustrated in the example above, accomplishes the following.

1) In an FET traveling-wave amplifier, gate-line loading determines the total gate periphery that can be used per stage [4]. With the present approach, the increased gate periphery per unit FET does not increase the gate-line loading. For the example above, although the device periphery is doubled, the gate-line attenuation, which is proportional to $r_g \omega^2 C_{gs}^2$, is in fact reduced by a factor of two. This approach thus makes it possible to increase significantly the total device periphery per gain stage.

2) In an FET, drain–source capacitance is smaller than gate–source capacitance. With this approach, drain–source capacitance is increased, while the effective gate–source capacitance is kept the same. This makes phase matching between the input and output lines easier.

3) Increased device periphery makes it possible to bring the optimum ac load line of each FET closer to the drain-line impedance for better power match. This, coupled by the fact that input and output power of the amplifier can be quadrupled when the periphery, hence the dc power requirement, is only doubled, should result in increased efficiency.

4) The capacitors in series with the FET gate–source capacitance act as capacitive voltage dividers, reducing the magnitude of the RF voltage swing at the gate terminal. A

reduction in voltage by half corresponds to a fourfold increase in input power-handling capability.

5) The capacitors added in series with the gate inputs can each be made different. Thus, it is possible to vary the amount of RF voltage sampled from the input line and, in this way, compensate for the gate-line attenuation. When all the gate capacitors are of equal value, the first cell would saturate before the rest of the cells due to this attenuation.

Different coupling capacitors along the gate line, however, lead to phase differences for signals passing through different FET's. Phase correction can be accomplished by varying the length of transmission-line sections connecting the drain terminals to the output transmission line.

Some of the advantages described above, such as the increased input power capability or reduced gate loading, can also be achieved by simply lowering the gate-line impedance level. To get a fourfold increase in input power, similar to the example given above, the gate-line impedance must be lowered to 12.5 Ω. For comparison, we have also considered this approach. At this input impedance level and with the same 4800-μm total periphery, gain which is virtually identical to the coupled capacitor case was obtained. However, the design had two disadvantages.

First, there is no way to compensate for gate-line attenuation to get equal FET cell excitation. Second, to go back to the 50-Ω impedance level, a transformer (4:1 ratio, in this case) would be required at the input port capable of operating over the bandwidth of the amplifier. The size, insertion loss, and interaction of the transformer with the amplifier mismatch rendered this approach unacceptable.

III. Design Example

A capacitively coupled traveling-wave amplifier concept has been applied to a traveling-wave amplifier design in the 2–8-GHz frequency band. A similar approach has also recently appeared in the literature with a 2–21-GHz design [7].

In our design example, a bandwidth of 4:1 was required. The highest frequency of operation was 8 GHz, which allowed a maximum periphery of about 2400 μm without the discrete gate capacitors. After the addition of the capacitors, the total periphery was increased to 4800 μm.

For a given total periphery, too few cells will require long gate transmission lines for a matched condition. When these lengths approach a quarter wavelength at the highest frequency of operation, the gate line is no longer an effective slow-wave structure. To minimize the number of interconnecting lines, the minimum number of cells should be used. Designs of 4, 6, and 8 cells were tried, with 6- and 8-cell designs yielding best results. The 6-cell design was chosen for simplicity and minimum chip area over the 8-cell design. The gate transmission-line sections are approximately $\lambda/8$ long at 8 GHz.

In an attempt to excite all cells equally, the gate-line attenuation can be compensated by increasing the values of the gate capacitors for cells farther down the gate line. There is a tradeoff here, however, as the gate-line attenuation for the higher frequencies is greater than that of the lower frequencies. A gate capacitor profile must be reached that allows approximately constant gate voltages that do not exceed $V_{in}/2$ at any frequency. The least attenuation is at the lowest frequency so the largest voltages along the gate line will exist at this frequency. This frequency of least attenuation is modified, however, by the input blocking capacitor, so that the frequency of least attenuation is typically elevated to midband. Because of this variation of attenuation with frequency, it is impossible to excite all the cells equally at all frequencies. The best that can be done is to excite all cells equally at midband, which results in slowly increasing excitation at low frequencies and slowly decreasing excitation at high frequencies along the gate line. The tapering of the capacitor values and the resultant voltage distribution along the gate line is shown in Fig. 4.

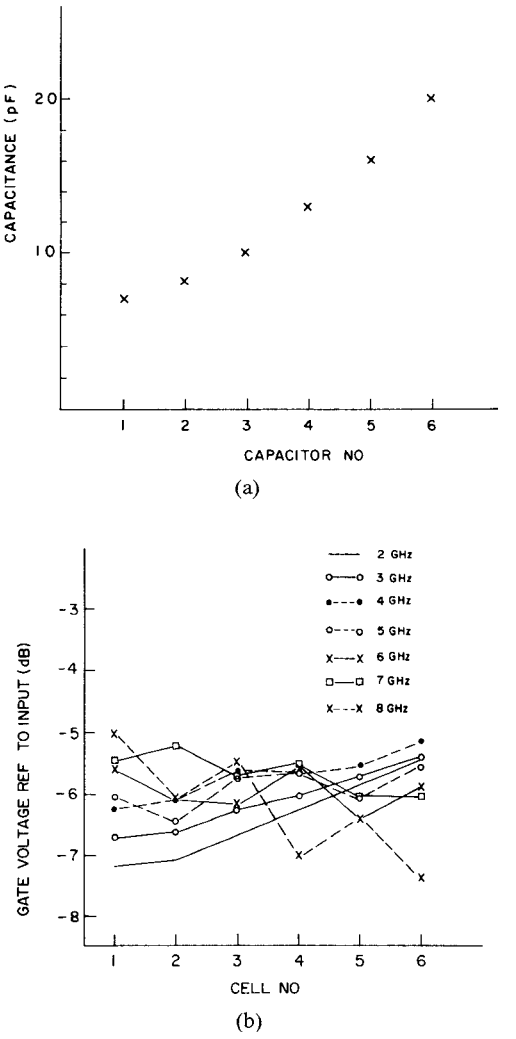

Fig. 4. (a) Capacitor tapering along the gate line to compensate for the gate-line attenuation. (b) Variation of the RF voltage at the FET gate terminals for each cell at various frequencies.

For the power amplifier design, drain-line impedance also becomes a consideration, for two reasons. First, gate–drain reverse breakdown limits the maximum peak-to-peak drain-line RF voltage swing, which is determined by the drain-line impedance for a given output power level.

TABLE I
MAXIMUM POWER EXPECTED (APPROXIMATELY) FOR 200 mW INPUT POWER (23 dBm)

DRAIN Ω	~ GAIN REDUCTION DUE TO LOWER DRAIN Ω (50 Ω REF.)	~ GAIN REDUCTION DUE TO DRAIN LINE ATTENUATION (dB)	(10.5 dB REF.) RESULTING APPROX. GAIN	POWER OUTPUT	POSSIBLE POWER OUT ASSUMING 19 V p-p MAX. SWING
50	0	-2.1 dB	8.4 dB	1.4 W	0.9 W
45	-.5 dB	-1.9 dB	8.07 dB	1.3 W	1.00 W
40	-.97 dB	-1.75 dB	7.78 dB	1.2 W	1.13 W
35	-1.55 dB	-1.56 dB	7.39 dB	1.1 W	1.29 W
30	-2.22 dB	-1.4 dB	6.88 dB	.98 W	1.51 W
25	-3 dB	-1.15 dB	6.36 dB	.86 W	1.81 W
20	-4 dB	-.94 dB	5.56 dB	.72 W	2.26 W

1. 10.5 dB ref in column 5 is derived from 4 × 600 gain of ~ 9.5 dB + 1 dB for drain line attenuation.
2. The assumption is made that dividing the input voltage in half and doubling the periphery results in the same gain. (Less drain losses)
3. Devices with V_{rb} = 25 V is assumed.

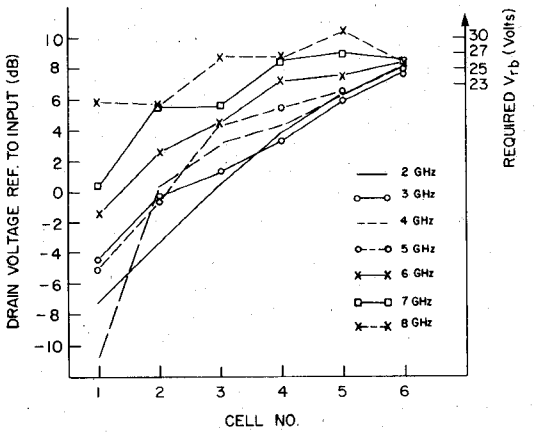

Fig. 5. Drain-voltage distribution at various frequencies.

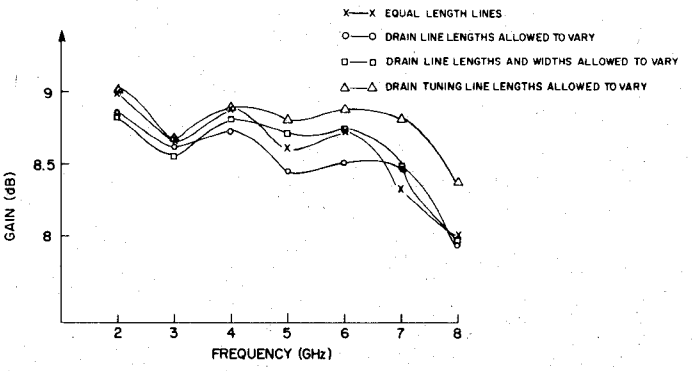

Fig. 6. Effects of adjusting drain lines and drain tuning lines to compensate for differing phaseshifts in each cell. Each case is an optimized result.

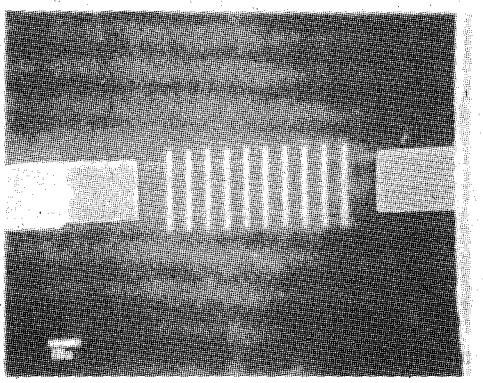

Fig. 7. SEM micrograph of a ten-open-gate FET used as a 2000-Ω resistor.

Second, with increased total device periphery, the drain-line attenuation becomes significant and needs to be minimized. The 6×400-μm single-stage design yields 10-dB gain. When dividing the input voltage in half and doubling the periphery to retain the gain, 10-dB gain was not achieved. The reason for this lies in the drain-line attenuation increase. When doubling the periphery per cell, C_{ds} and g_d are doubled. This increased loading causes a gain reduction of about 2 dB at the 50-Ω level. Reducing the impedance level of the drain line would reduce the effect of this loading.

The above two reasons prompted a study of operating into a lower drain Z_0. From the gain expression, it is clear that lowering the input or output impedance reduces gain directly in proportion to the impedance reduction. An optimum impedance level was determined by considering all the above variables. The gain reduction due to the lower drain Z_0 is a stronger function than the gain increase due to less drain-line attenuation. Therefore, lowering drain Z_0 will decrease gain in all cases. This is shown in Table I. The tradeoff between reduced gain and increased power seems optimum at the 40-Ω drain impedance level. It was decided that transforming this to 50 Ω was not worthwhile, and a 50-Ω drain line would be maintained with its associated 8.4-dB total gain. The limiting factor on power output now is clearly the breakdown voltage of the devices used. The drain voltage distribution is shown in Fig. 5.

The gain was optimized to the 8.5-dB level by correcting for the phase differences across each cell due to the graded profile of the gate capacitors. Several methods of accomplishing this were looked at, including decreasing gate- and drain-line lengths, but the best method was phase alignment within each cell by adjusting the length of the drain tuning lines as can be seen in Fig. 6.

The transmission lines connecting each cell remain equal, although they are different lengths and widths for gate and drain.

IV. EXPERIMENTAL RESULTS

The circuit described above has been fabricated on a 100-μm-thick GaAs substrate.

The design uses six FET's, each with 800-μm gate periphery with nominal 1-μm gate lengths. The channel is 1×10^{17} cm^{-3} doped VPE material. Each FET gate is individually biased through 2 KΩ resistors connected to a common-gate bias bus. These high-value resistors and the 35-Ω gate- and drain-line matching resistors are realized using the floating-gate FET resistors shown in Fig. 7. The thin-film capacitors use 0.5-μm-thick Si_3N_4 as the dielectric medium. In this way, the fabrication process is quite simplified, to no more than the regular FET process plus plasma-assisted chemical vapor deposition of silicon nitride

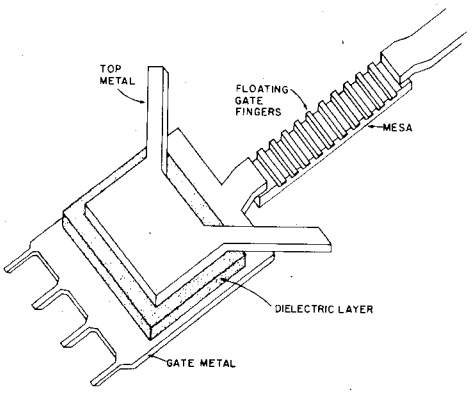

Fig. 8. Schematic illustration of the gate-biasing arrangement. The dimensions are not to scale and some details are omitted for simplification.

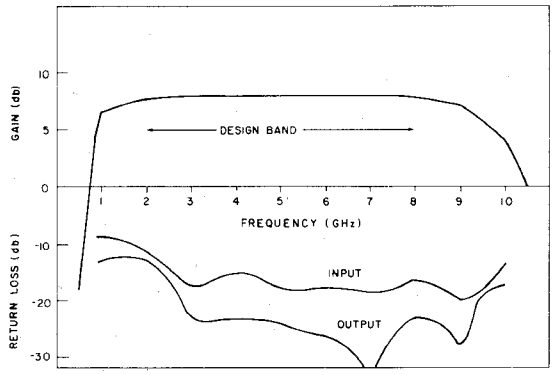

Fig. 9. Predicted performance of the 2–8-GHz amplifier.

film. The thin-film capacitor and the floating resistor are configured as shown in Fig. 8 to eliminate dc/RF crossovers.

The predicted gain and return-loss performance of the amplifier is shown in Fig. 9. The gain is very flat and slightly less than 8 dB in the 2–8-GHz design band. The return loss is 12 dB at 2 GHz, and better than 15 dB above 2.5 GHz.

The finished chip is shown in Fig. 10. Its dimensions are 3×3.1 mm. The top plates of the capacitors on the gate pads are proportional to their capacitance. Notice the increase in the area of the top plates as we move along the gate line away from the input terminal. This increase compensates for the attenuation of the gate line.

Typical small-signal measured performance of the amplifier in the 0.5–10-GHz frequency band is shown in Fig. 11. The gain is lower than the design by 1.2 dB at the low end and by 2.6 dB at the high end of the band. Input and output return loss is very close to predictions. Power performance of the amplifier is shown in Fig. 12. Near 1-dB compression, the power output is 30 ± 0.5 dBm with 5 dB of gain across the 2–8-GHz band.

Measured amplifier efficiency varies between 5.2 to 8.5 percent. This is about half of what is expected. We find that this discrepancy is partially due to the dc voltage drop along the on-chip dc-bias circuitry and partially due to the loading on the output drain line.

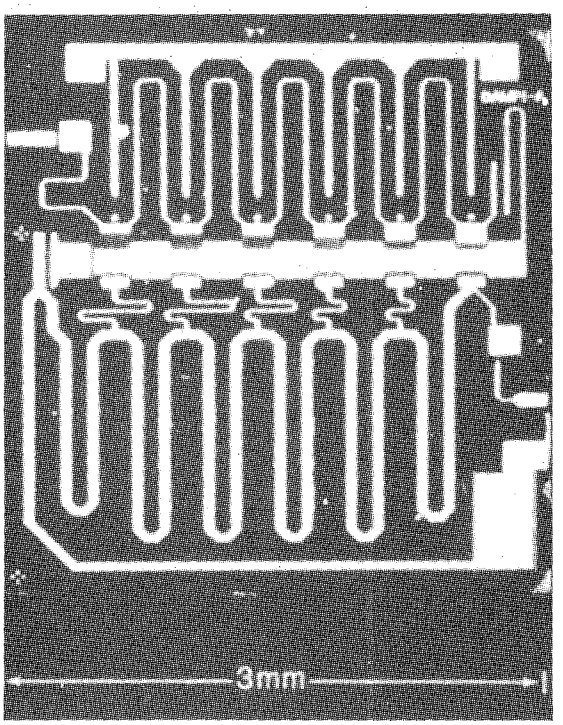

Fig. 10. The finished chip.

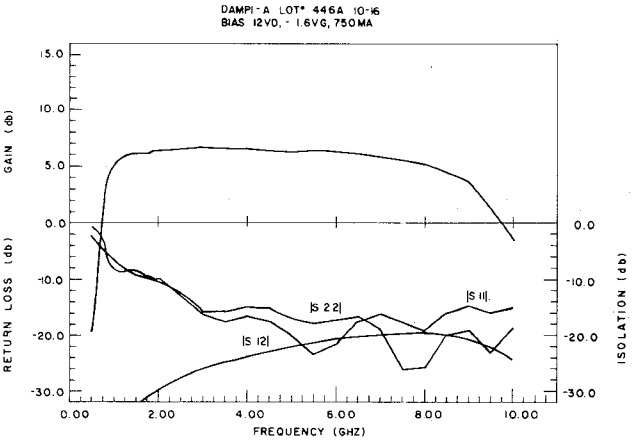

Fig. 11. Small-signal performance of a typical amplifier.

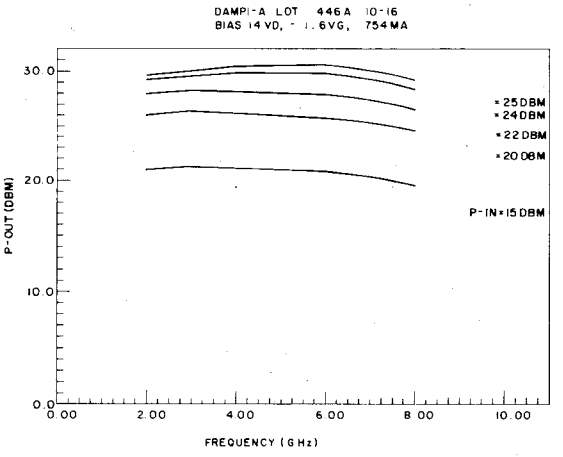

Fig. 12. Measured power performance of the amplifier.

V. Conclusion

A new circuit approach to increase the power amplification capability of distributed or traveling-wave amplifiers has been introduced. The validity of the approach has been demonstrated by designing a 1-W amplifier in the 2–8-GHz frequency band.

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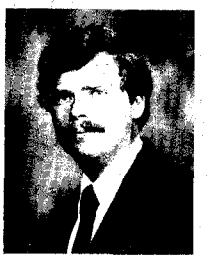

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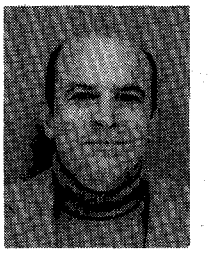

Robert Mozzi received a B.S. degree in physics from Villanova College, Villanova, PA, in 1953 and an M.S. degree in physics from the University of Pittsburgh, PA, in 1955.

He was employed as an Analytical Physicist at Pratt and Whitney Aircraft from 1955 to 1957. In December 1957, he joined the Raytheon Research Division where he has worked on ferrite structures, including cation distribution in spinels and other structural problems associated with ferrite materials. He developed improved techniques for studying thin films using total external reflection of X-rays. From 1963 to 1967, he attended the Massachusetts Institute of Technology, Cambridge, under a Raytheon advanced study grant. His studies at MIT culminated in a thesis on an X-ray diffraction study of the structure of glass. He was awarded his Ph.D. degree in physics in February 1968. After returning to the Research Division in October 1967, he was responsible for the application of X-ray techniques, including X-ray topography, to the study of imperfections in single crystals. In addition to qualitative evaluations of the degree of perfection of a variety of single crystals and epitaxially grown thin films, he carried out more detailed studies of the structural damage induced by impurity diffusion in silicon and InSb crystals.

Larry K. Hanes received the B.S. degree in physics with honors from North Texas State University, Denton, TX, in 1976. He received the M.S. degree in 1977 and the Ph.D. degree in 1982, also in physics, from North Texas State.

From 1976 to 1980, he was a Research Assistant working on quantum electronics and solid-state physics at North Texas State. His thesis research investigated the effects of hot electrons in InSb excited by a carbon monoxide laser on magneto-transport phenomena and photoconductivity. His research involved the design, construction, and use of a continuous-wave carbon monoxide laser and accessory equipment for the measurements of laser-induced changes in the electrical conductivity and Shubnikov–de Haas effect. He joined the Raytheon Research Division in 1980, where he has been working in the Semiconductor Laboratory. His responsibilities include the design of GaAs monolithic microwave integrated-circuits mask layouts.